

LP3997

Micropower 250mA CMOS LDO Regulator with Error Flag / Power-On-Reset

General Description

The LP3997 regulator is designed to meet the requirements of portable, battery-powered systems, providing accurate output voltage, low noise, and low quiescent current. The LP3997 provides 3.3V output at up to 250mA load current. The chip architecture is capable of providing output voltages as low as 0.8V. When switched in shutdown mode, the power consumption is virtually zero.

The LP3997 is designed to be stable with space saving ceramic output capacitor as small as 1 μ F.

The LP3997 also includes an out-of-regulation error flag. When the output is more than 5% below its nominal voltage, the error flag sets to low. If a capacitor is connected to device's delay pin, a delayed power-on reset signal will be generated.

Features

- Low, 140mV, Dropout at 250mA Load.
- Stable with Ceramic Capacitor.

- Low Noise, with Bypass Capacitor.
- Less than 80 μ A Typical I_Q at 250mA.
- Virtually Zero I_Q (Disabled).
- Thermal and Short Circuit Protection.
- 3.3V Output.

For other voltage options contact your NSC sales office

Package

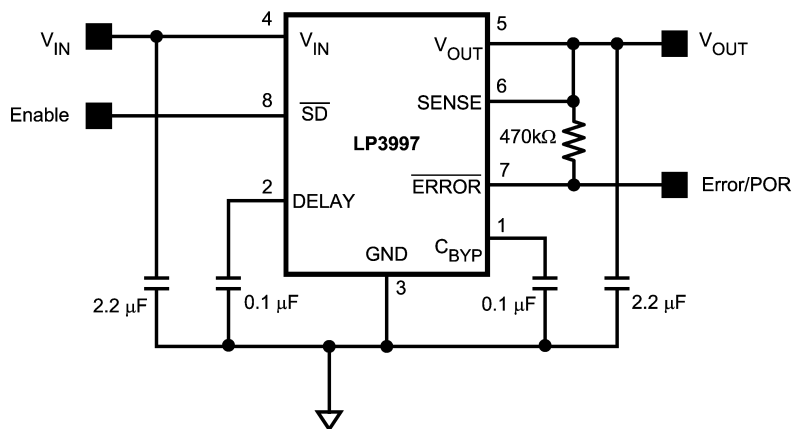
8 Lead MSOP

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Applications

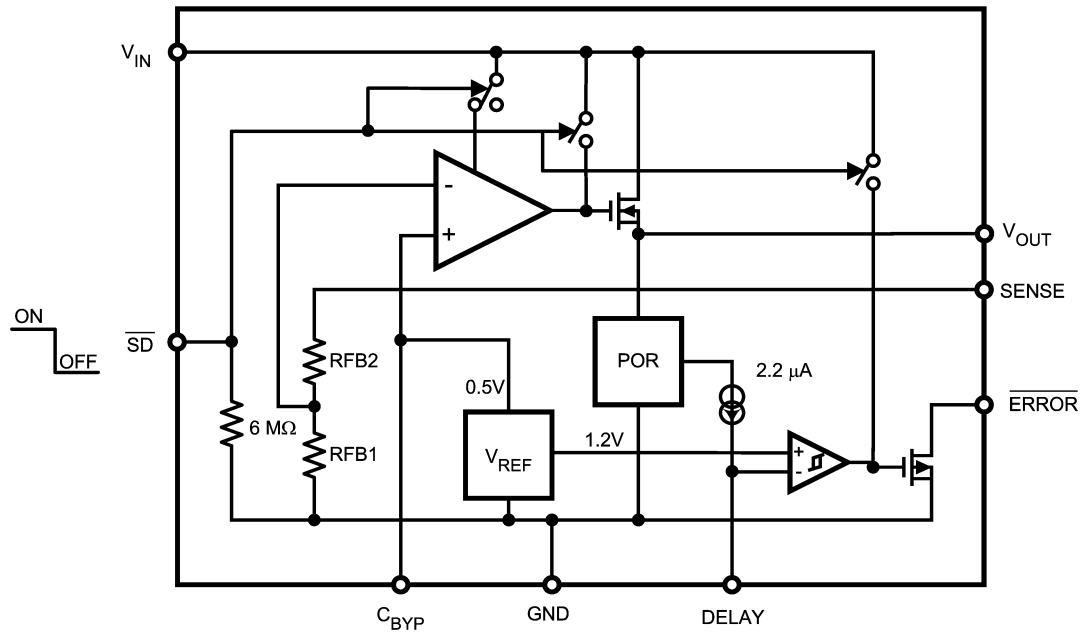
- Portable Consumer Electronics
- Cellular Handsets
- Laptop and Palm Computers
- PDA's
- Digital Cameras

Typical Application Circuit



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Functional Block Diagram

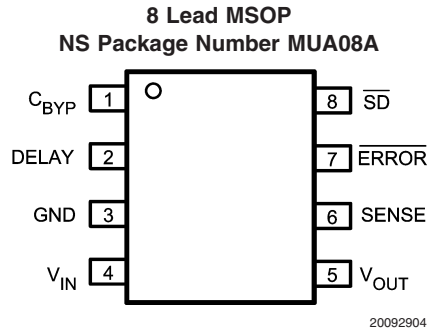


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Pin Descriptions

Pin #	Name	Description
1	C_{BYP}	Noise bypass pin. For low noise applications a 0.1 μ F or larger ceramic capacitor should be connected from this pin to ground. This will also improve PSSR.
2	DELAY	A capacitor connected from this pin to ground will allow a delayed power-on-reset signal at the ERROR (pin 7) output. See Applications Information.
3	GND	Ground pin. Local ground for C_{BYP} , C_{IN} , C_{OUT} and C_{DELAY} .
4	V_{IN}	Input supply pin. Connect C_{IN} between this pin and GND.
5	V_{OUT}	Output voltage, Connect C_{OUT} between this pin and ground.
6	SENSE	Connect this pin to V_{OUT} (pin 5). For best performance the connection should be made as close to the load as possible.
7	\overline{ERROR}	This open drain output is an error flag output which goes low when V_{OUT} drops 5% below its nominal voltage. This pin also provides a power-on-reset signal if a capacitor is connected to the DELAY pin.
8	\overline{SD}	Shutdown. Disables the regulator when less than 0.4V is applied. Enables the regulator when greater than 0.9V. The Shutdown pin is pulled down internally by a 6M Ω resistor.

Connection Diagram



Ordering Information

For MSOP Package

Output Voltage (V)	Grade	LP3997 Supplied as 1000 Units, Tape and Reel	LP3997 Supplied as 3500 Units, Tape and Reel	Package Marking
3.3	STD	LP3997MM-3.3	LP3997MMX-3.3	SAKB

Absolute Maximum Ratings

(Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Input Voltage	-0.3 to 6.5V
Output Voltage	-0.3 to ($V_{IN} + 0.3V$) with 6.5V (max)
\overline{SD} Input Voltage	-0.3 to ($V_{IN} + 0.3V$) with 6.5V (max)
Junction Temperature	150°C
Lead/Pad Temp.	
MSOP	260°C
Storage Temperature	-65 to 150°C
Continuous Power Dissipation Internally Limited (Note 3)	
ESD (Note 4)	
All Pins Except C_{BYP}	
Human Body Model	2KV

Machine Model	200V
C_{BYP} Pin	
Human Body Model	1KV
Machine Model	100V

Operating Ratings

(Note 1)

Input Voltage	2V to 6V
Junction Temperature	-40°C to 125°C
Ambient Temperature T_A Range	-40°C to 85°C

(Note 5)

Thermal Properties

(Note 1)

Junction To Ambient Thermal Resistance (Note 6)	
θ_{JA} (MSOP)	210°C/W

Electrical Characteristics

Unless otherwise noted, $\overline{SD} = 950mV$, $V_{IN} = V_{OUT} + 1.0V$, $C_{IN} = 2.2 \mu F$, $I_{OUT} = 1 mA$, $C_{OUT} = 2.2 \mu F$ and $C_{BYP} = 0.1 \mu F$. Typical values and limits appearing in normal type apply for $T_J = 27^\circ C$. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to +125°C. (Note 12)

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
V_{IN}	Input Voltage			2	6	V
ΔV_{OUT}	Output Voltage Tolerance	Over full line and load regulation.		-1.5	+1.5	%
	Line Regulation Error	$V_{IN} = (V_{OUT(NOM)} + 1.0V)$ to 6.0V, $I_{OUT} = 1mA$	0.02	-3	+3	%/V
	Load Regulation Error	$I_{OUT} = 1mA$ to 250mA	20		80	$\mu V/mA$
V_{DO}	Dropout Voltage	$I_{OUT} = 250mA$ (Note 7)	140		400	mV
I_{LOAD}	Load Current	(Notes 8, 9)		0		μA
I_Q	Quiescent Current	$\overline{SD} = 950mV$, $I_{OUT} = 0mA$	55		100	μA
		$\overline{SD} = 950mV$, $I_{OUT} = 250mA$	80		150	
		$\overline{SD} = 0.4V$	0.01		0.5	
I_{SC}	Short Circuit Current Limit	(Note 10)	600		1000	mA
I_{OUT}	Maximum Output Current			250		mA
PSRR	Power Supply Rejection Ratio	$C_{BYP} = 0.1\mu F$	$f = 1kHz$, $I_{OUT} = 1mA$ to 150mA	61		dB
			$f = 10kHz$, $I_{OUT} = 150mA$	55		
		Without C_{BYP}	$f = 1kHz$, $I_{OUT} = 1mA$ to 150mA	61		
			$f = 10kHz$, $I_{OUT} = 150mA$	39		
e_n	Output noise Voltage (Note 9)	BW = 10Hz to 100kHz, $V_{IN} = V_{OUT(nom)} + 1V$	w/o C_{BYP}	180		μV_{RMS}
			$C_{BYP} = 0.1\mu F$	100		

Electrical Characteristics (Continued)

Unless otherwise noted, $\overline{SD} = 950\text{mV}$, $V_{IN} = V_{OUT} + 1.0\text{V}$, $C_{IN} = 2.2\ \mu\text{F}$, $I_{OUT} = 1\ \text{mA}$, $C_{OUT} = 2.2\ \mu\text{F}$ and $C_{BYP} = 0.1\ \mu\text{F}$. Typical values and limits appearing in normal type apply for $T_J = 27^\circ\text{C}$. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to $+125^\circ\text{C}$. (Note 12)

Symbol	Parameter	Conditions	Typ	Limit		Units	
				Min	Max		
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature	150			$^\circ\text{C}$	
		Hysteresis	10				
Shutdown Control Characteristics							
$I_{\overline{SD}}$	Maximum Input Current at \overline{SD} Input	$\overline{SD} = 0.0\text{V}$	0.01			μA	
		$\overline{SD} = 6\text{V}$ (Note 11)	1				
V_{IL}	Low Input Threshold	$V_{IN} = 2\text{V}$ to 6V			0.4	V	
V_{IH}	High Input Threshold	$V_{IN} = 2\text{V}$ to 6V			0.95	V	
Error Flag Characteristics							
V_{TH}	Power Good Trip Threshold	V_{IN} Rising	95	91	99	$\%V_{OUT}$	
V_{HYST}	Hysteresis	V_{IN} Rising or Falling	2.5			$\%V_{OUT}$	
V_{OL}	Error Error Output Output low Voltage	$I_{SINK} = 2\text{mA}$	0.1		0.4	V	
I_{OFF}	Error Output High Leakage	$\overline{ERROR} = V_{OUT(NOM)}$	10		2000	nA	
I_{DELAY}	Delay Pin Current Source	$V_{OUT} > 95\% V_{OUT(NOM)}$	2.2	1.2	3	μA	
Timing Characteristics							
t_{ON}	Turn On Time (Note 9)	To 95% Level	w/o C_{BYP}	150		250	μs
			$C_{BYP} = 0.1\ \mu\text{F}$	2			ms
Transient Response	Line Transient Response $ \delta V_{OUT} $	$T_{rise} = T_{fall} = 30\ \mu\text{s}$ (Note 9) $\delta V_{IN} = 600\text{mV}$	w/o C_{BYP}	40			mV (pk - pk)
			$C_{BYP} = 0.1\ \mu\text{F}$	4			
	Load Transient Response $ \delta V_{OUT} $	$T_{rise} = T_{fall} = 1\ \mu\text{s}$ (Note 9) $I_{OUT} = 1\text{mA}$ to 150mA	70		80	mV	

Note 1: Absolute Maximum Ratings are limits beyond which damage can occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All Voltages are with respect to the potential at the GND pin.

Note 3: Internal thermal shutdown circuitry protects the device from permanent damage.

Note 4: The human body model is 100pF discharged through a 1.5k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 5: The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)} = 125^\circ\text{C}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

Note 6: Junction to ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible, special care must be paid to thermal dissipation issues in board design.

Note 7: Dropout voltage is defined as the voltage difference between input and output when the output voltage drops 100mV below its nominal value.

Note 8: The device maintains the regulated output voltage without the load.

Note 9: This electrical specification is guaranteed by design.

Note 10: Short circuit current is measured on the input supply line at the point when the short circuit condition reduces the output voltage to 5% of its nominal value.

Note 11: \overline{SD} Pin has 6M Ω typical, resistor connected to GND.

Note 12: All limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production at $T_J = 25^\circ\text{C}$ or correlated using Statistical Quality Control methods. Operation over the temperature specification is guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

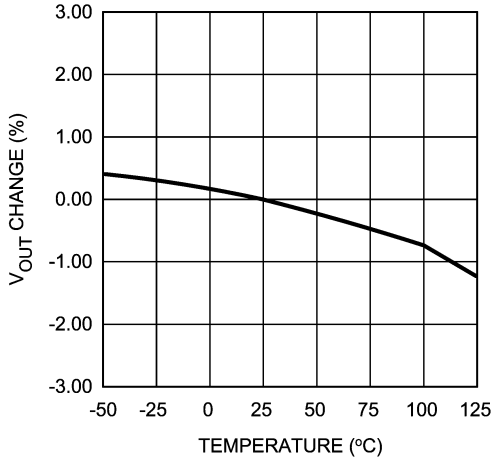
Output Capacitor, Recommended Specifications

Symbol	Parameter	Conditions	Typ	Limit		Units
				Min	Max	
C_o	Output Capacitor	Capacitance(Note 13)	2.2	0.7		μF
		ESR		5	500	m Ω

Note 13: The capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor type is X7R. However, dependent on application, X5R, Y5V, and Z5U can also be used. (See capacitor characteristics section in Application Hints)

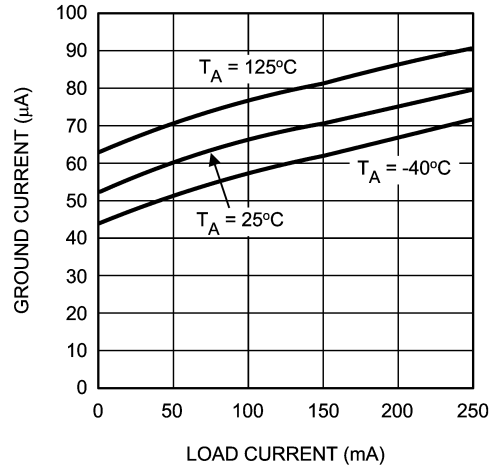
Typical Performance Characteristics. Unless otherwise noted, $SD = 950mV$, $V_{IN} = V_{OUT} + 1.0V$, $C_{IN} = 2.2 \mu F$, $I_{OUT} = 1 \text{ mA}$, $C_{OUT} = 2.2 \mu F$ and $C_{BYP} = 0.1 \mu F$. Typical values and limits appearing in normal type apply for $T_J = 27^\circ C$. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to $+125^\circ C$.

Output Voltage Change vs Temperature



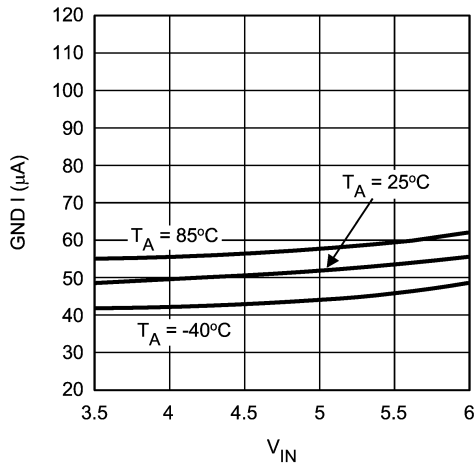
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Ground Current vs Load Current



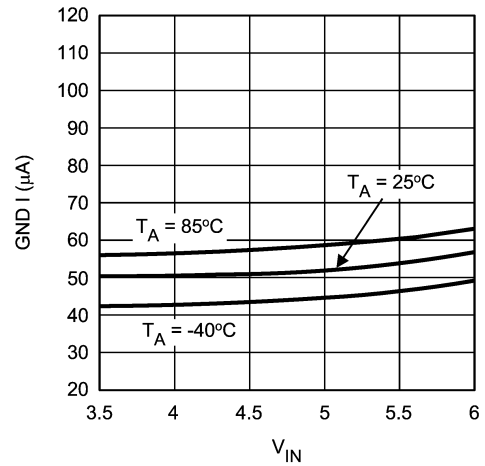
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Ground Current vs V_{IN} , $I_{LOAD} = 0mA$



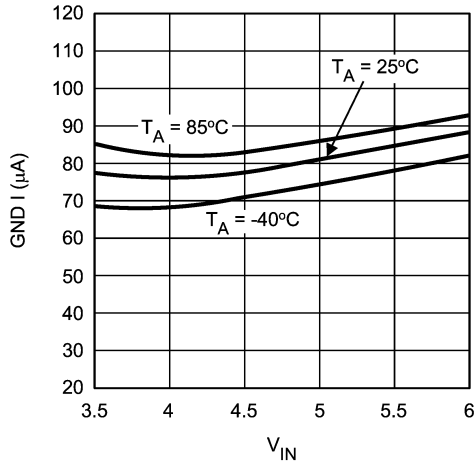
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Ground Current vs V_{IN} , $I_{LOAD} = 1mA$



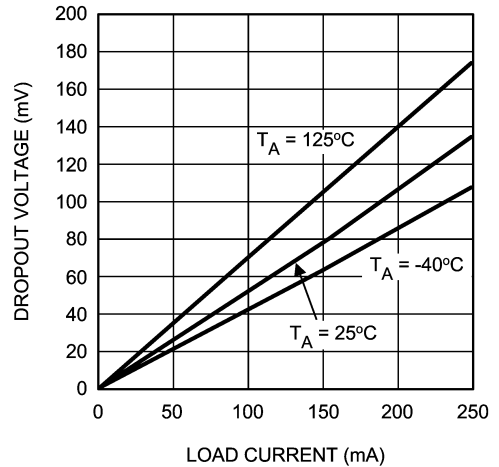
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Ground Current vs V_{IN} , $I_{LOAD} = 250mA$



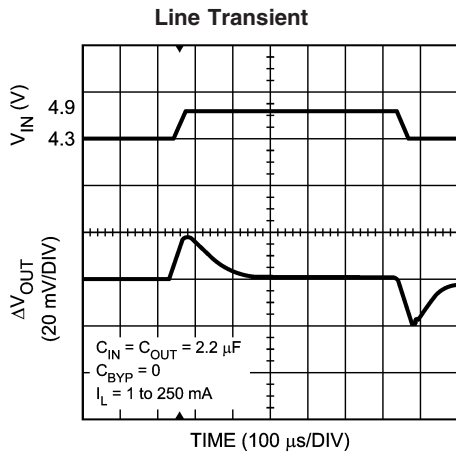
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Dropout Voltage vs Load Current

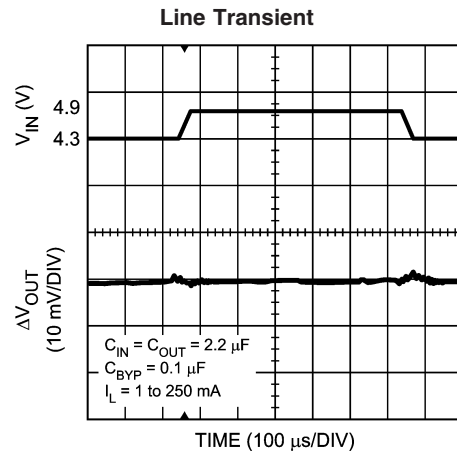


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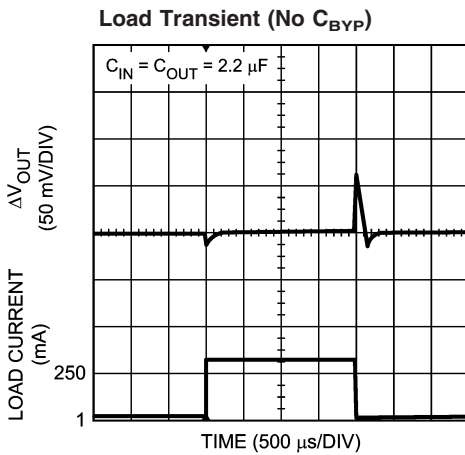
Typical Performance Characteristics. Unless otherwise noted, $SD = 950mV$, $V_{IN} = V_{OUT} + 1.0V$, $C_{IN} = 2.2 \mu F$, $I_{OUT} = 1 \text{ mA}$, $C_{OUT} = 2.2 \mu F$ and $C_{BYP} = 0.1 \mu F$. Typical values and limits appearing in normal type apply for $T_J = 27^\circ C$. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to $+125^\circ C$. (Continued)



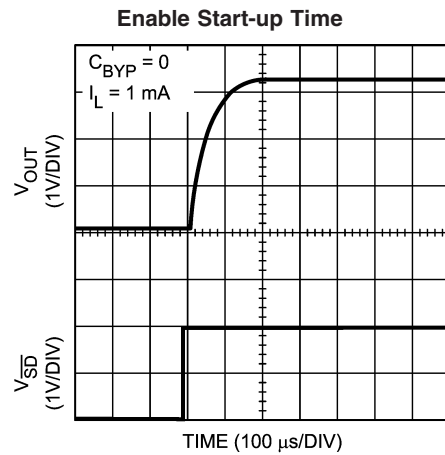
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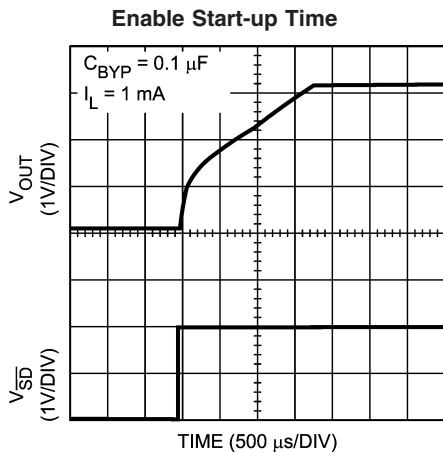
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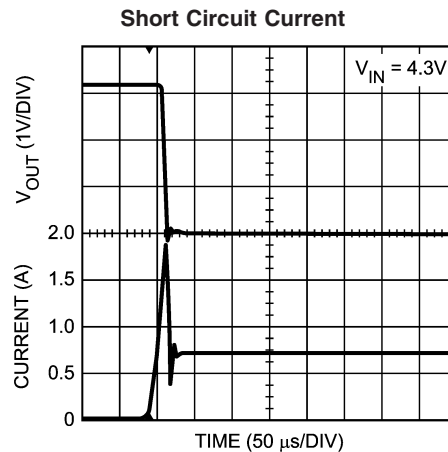
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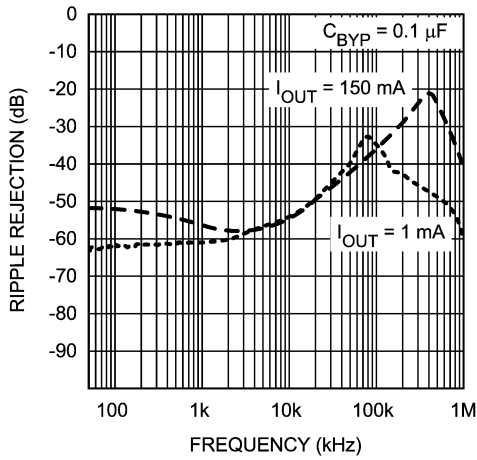
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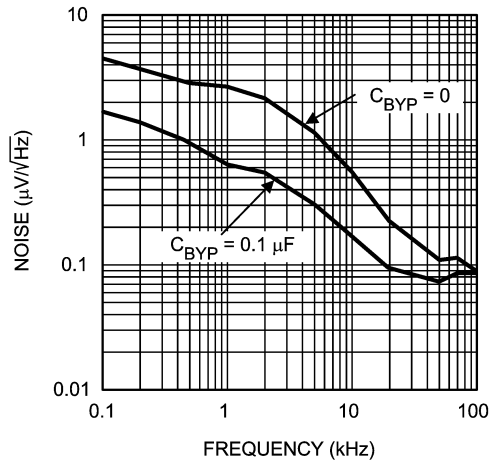
Typical Performance Characteristics. Unless otherwise noted, $\overline{SD} = 950\text{mV}$, $V_{IN} = V_{OUT} + 1.0\text{V}$, $C_{IN} = 2.2 \mu\text{F}$, $I_{OUT} = 1 \text{ mA}$, $C_{OUT} = 2.2 \mu\text{F}$ and $C_{BYP} = 0.1 \mu\text{F}$. Typical values and limits appearing in normal type apply for $T_J = 27^\circ\text{C}$. Limits appearing in **boldface** type apply over the full temperature range for operation, -40 to $+125^\circ\text{C}$. (Continued)

Power Supply Rejection Ratio



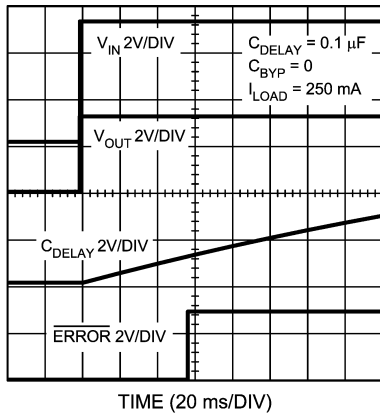
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Noise Spectrum



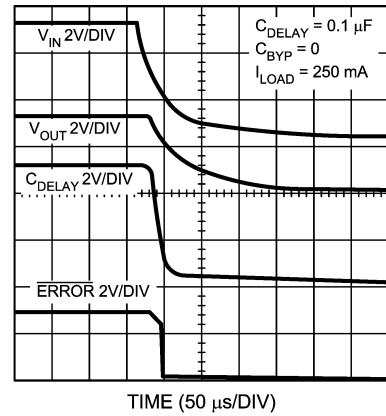
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Turn-On Sequence



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Turn-Off Sequence



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Applications Information

External Capacitors

In common with most regulators, the LP3997 requires the inclusion of external capacitors.

V_{IN}

An input capacitor is required for stability. It is recommended that a minimum of 1.0 μ F capacitor is connected between the LP3997 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: To ensure stable operation it is essential that good PCB design practices are employed to minimize ground impedance and keep input inductance low. If these conditions cannot be met, or if long wire leads are used to connect the battery or other power source to the LP3997, then it is recommended to increase the input capacitor to at least 2.2 μ F. Also, tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be guaranteed by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain \approx 1.0 μ F over the entire operating temperature range.

V_{OUT}

V_{OUT} is the output voltage of the regulator. Connect capacitance (minimum 1.0 μ F) to ground from this pin. To ensure stability the capacitor must meet the minimum value for capacitance and have an ESR in the range 5m Ω to 500m Ω . Ceramic X7R types are recommended. If an output capacitor larger than 4.7 μ F is fitted then checks on in-rush current, transient performance and stability, should be made.

SENSE

SENSE is used to sense the output voltage. Connect sense to V_{OUT}

SHUTDOWN

\overline{SD} controls the turning on and off of the LP3997. V_{OUT} is guaranteed to be on when the voltage on the \overline{SD} pin is greater than 0.95V. V_{OUT} is guaranteed to be off when the voltage on the \overline{SD} pin is less than 0.4V.

ERROR

ERROR is an open drain output which is set low when V_{OUT} is more than 5% below its nominal value. An external pull up resistor is required on this pin. When a capacitor is connected from DELAY to GROUND, the error signal is delayed (see DELAY section). This delayed error signal can be used as the power-on reset signal for the application system. The ERROR pin is disconnected when not used.

DELAY

A capacitor from DELAY to GROUND sets the time delay for ERROR changing from low to high state. The delay time is set by the following formula.

$$t_{DELAY} = \frac{V_{TH(DELAY)} \times C_{DELAY}}{I_{DELAY}}$$

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$V_{TH(DELAY)}$ is nominally 1.2V.

The DELAY pin should be open circuit if not used.

C_{BYP}

For low noise application, connect a high frequency ceramic capacitor from C_{BYP} to ground. A 0.01 μ F to 0.1 μ F X5R or X7R is recommended. This capacitor is connected directly to high impedance node in the band gap reference circuit. Any significant loading on this node will cause a change in the regulated output voltage. For this reason, DC leakage current from this pin must be kept as low as possible for best output voltage accuracy.

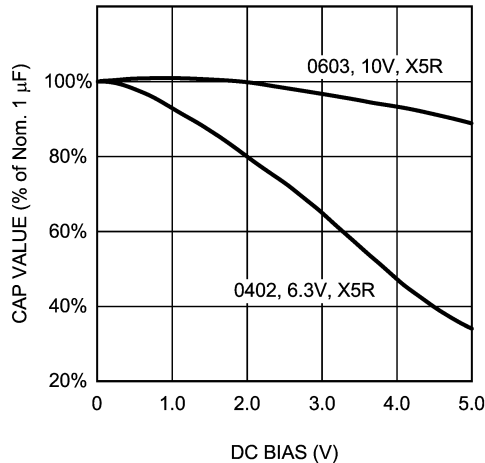
CAPACITOR CHARACTERISTICS

In common with most regulators, the LP3997 requires external capacitors for regulator stability. The LP3997 is specifically designed for portable applications requiring minimum board space and can use capacitors in the range 1 μ F to 4.7 μ F. These capacitors must be correctly selected for good performance. Ceramic capacitors are the smallest, least expensive and have the lowest ESR values (which makes them best for eliminating high frequency noise). The ESR of a typical 1 μ F ceramic capacitor is in the range of 20 m Ω to 40 m Ω , which easily meets the ESR requirement for stability by the LP3997. These capacitors must be correctly selected to ensure good performance of the LP3997.

For both input and output capacitors careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly dependant on the conditions of operation and capacitor type.

In particular the output capacitor selection should take account of all the capacitor parameters to ensure that the specification is met within the application. Capacitance value can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size with smaller sizes giving poorer performance figures in general. As an example *Figure 1* shows a typical graph showing a comparison of capacitor case sizes in a Capacitance versus DC Bias plot. As shown in the graph, as a result of the DC Bias condition, the capacitance value may drop below the minimum capacitance value given in the recommended capacitor table (0.7 μ F in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions as some capacitor sizes (e.g. 0402) may not be suitable in the actual application.

Applications Information (Continued)



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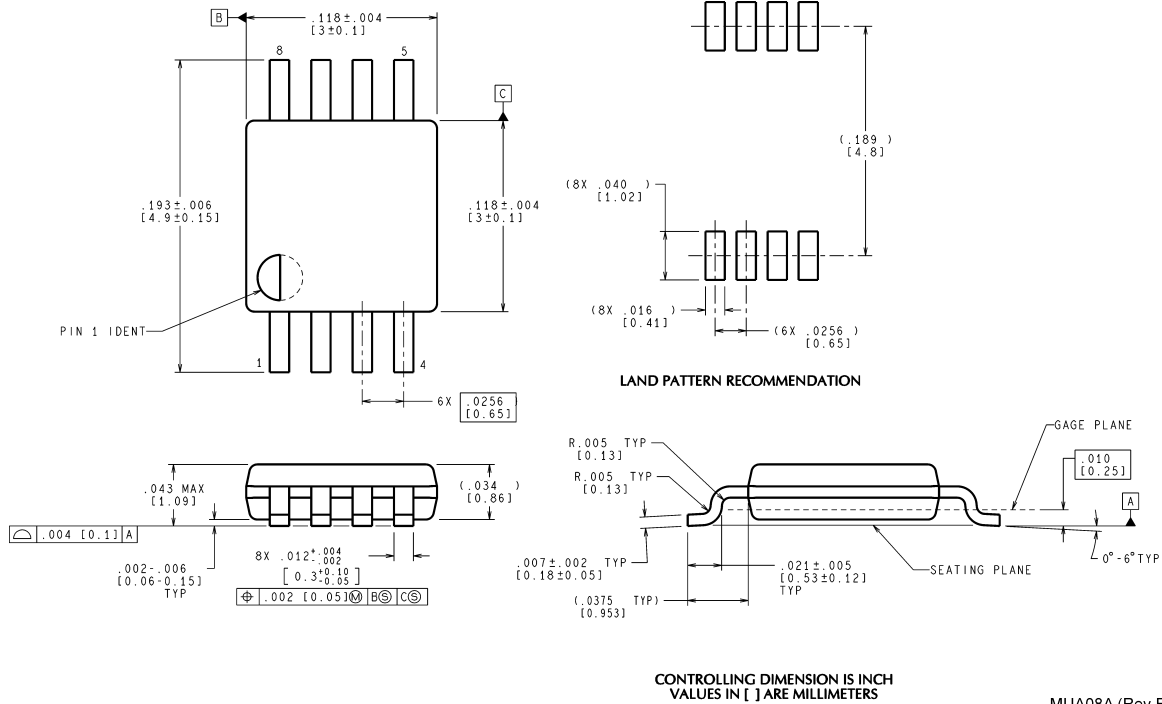
FIGURE 1. Graph Showing a Typical Variation in Capacitance vs DC Bias

The value of ceramic capacitors can vary with temperature. The capacitor type X7R, which operates over a temperature range of -55°C to $+125^{\circ}\text{C}$, will only vary the capacitance to within $\pm 15\%$. The capacitor type X5R has a similar tolerance over a reduced temperature range of -55°C to $+85^{\circ}\text{C}$. Most large value ceramic capacitors, larger than $1\mu\text{F}$ are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature goes from 25°C to 85°C . Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C .

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the $1\mu\text{F}$ to $4.7\mu\text{F}$ range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to -40°C , so some guard band must be allowed.

Physical Dimensions inches (millimeters) unless otherwise noted



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